REMARKS

Claims 25-32 and 44-47 are pending in the present application.

In the office action mailed June 10, 2005 (the "Office Action"), claims 25, 27, 29, 30, 31, 44, 46, and 47 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,124,660 to Cilingiroglu (the "Cilingiroglu patent"). The Examiner also rejected claim 26 under 35 U.S.C. 103(a) as being unpatentable over the Cilingiroglu patent in view of U.S. Patent No. 6,242,941 to Vest *et al.* (the "Vest patent"), and rejected claim 45 under 35 U.S.C. 103(a) as being unpatentable over Cilingiroglu in view of U.S. Patent No. 6,714,031 to Seki (the "Seki patent").

Claims 25, 27, and 28 have been amended to recite "data terminals" instead of "signal terminals," so that "data terminals" is used consistently throughout claims 25-32.

The Cilingiroglu patent is directed to a test system for testing the continuity of pins of an integrated circuit ("IC") device and a circuit board to which the IC device is mounted. As shown in Figure 1, an electrode 106 coupled to an oscillator 104 is positioned in proximity to the IC 110. The alternating signal that is applied to the electrode 106 induces currents in the pins of the IC 110, as explained at col. 3, line 48-col. 4, line 3 and with reference to Figures 2 and 3. A pin under test 112 is coupled to an ammeter 116 through a circuit board trace 114. The ammeter 116 is used to measure whether the induced current can be detected from the circuit board trace 114. If a sufficient level of current is detected, then the pin under test 112 is electrically coupled to the circuit board trace 114. Conversely, if the sufficient level of current is not detected, the pin under test 112 is considered to be open, or not electrically coupled to the circuit board trace 114. The continuity of all of the pins of the IC 110 to the respective circuit board trace can be tested by switching among the pin under test and determining if a sufficient level of current is detected at each pin.

Claims 25 and 44 as amended are patentably distinct from the Cilingiroglu patent because the Cilingiroglu patent fails to disclose the combination of limitations recited by the respective claims. For example, the Cilingiroglu patent fails to disclose capacitively coupling a test plate integrated in the integrated circuit to a plurality of data terminals at which data signals are received. As previously discussed, the Cilingiroglu patent describes using an external electrode 106 to test the electrical continuity between the IC 110 and a circuit board, represented

by circuit board trace 114 in Figure 1. This is illustrated in Figures 1-3, with electrode 106 positioned over the IC 110. As described in the Cilingiroglu patent, an insulator 108 may be placed between the electrode 106 and the IC 110, further confirming that the electrode 106 is not integrated in the IC 106. *See* col. 3, lines 26-28. Figure 4 illustrates an electrode 420 positioned over (i.e., externally) the IC package 402 and Figure 5 illustrates positioning electrodes 502-504 of board 501 over the ICs 506, 508, and 510 of the printed circuit board 500.

For the foregoing reasons, claims 25 and 44 are patentably distinct from the Cilingiroglu patent. Claims 27, 29, 30, and 31, which depend from claim 25, and claims 46 and 47, which depend from claim 44, are similarly patentably distinct based on their dependency from respective allowable base claims. That is, each of the dependent claims further narrows the scope of the claim from which it depends, and consequently, if a claim is dependent from an allowable base claim, the dependent claim is also allowable. Therefore, the rejection of claims 25, 27, 29, 30, 31, 44, 46, and 47 under 35 U.S.C. 102(b) should be withdrawn.

As previously mentioned, claim 26 has been rejected under 35 U.S.C. 103(a) as being unpatentable over the Cilingiroglu patent in view of the Vest patent and claim 45 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Cilingiroglu in view of the Seki patent. Claims 26 and 45 are patentable due to their dependency from allowable base claims 25 and 44, respectively, as previously discussed. Moreover, the combined teachings of the Cilingiroglu patent and the Vest patent fail to teach or suggest the combination of limitations recited by claim 26 and the combined teachings of the Cilingiroglu patent and the Seki patent fail to teach or suggest the combination of limitations recited by claim 45. The Vest patent has been cited by the Examiner as disclosing placing remaining data terminals of a plurality in a high-impedance state and the Seki patent has been cited by the Examiner as disclosing a test transmitter that is a buffer circuit. *See* the Office Action at pages 4 and 5. Assuming for the sake of argument that the Examiner's characterization of the Vest and Seki patents is accurate, the teachings of the respective patents fail to make up for the deficiencies of the Cilingiroglu patent previously discussed with respect to claims 25 and 44.

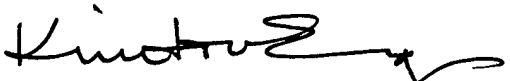
For the foregoing reasons, claim 26 is patentable over the Cilingiroglu patent in view of the Vest patent and claim 45 is patentable over the Cilingiroglu patent in view of the

Seki patent. Consequently, the rejection of claims 26 and 45 under 35 U.S.C. 103(a) should be withdrawn.

All of the claims pending in the present application are in condition for allowance. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Kimton N. Eng
Registration No. 43,605
Telephone No. (206) 903-8718

KNE:ajs

Enclosures:
Postcard
Fee Transmittal Sheet (+ copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

h:\ip\clients\micron technology\1300\501317.02\501317.02 amendment.doc